

# Cubic Phase GaN on Nano-grooved Si (100) via Maskless Selective Area Epitaxy

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A method of forming cubic phase (zinc blende) GaN (referred as c-GaN) on a CMOS-compatible on-axis Si (100) substrate is reported. Conventional GaN materials are hexagonal phase (wurtzite) (referred as h-GaN) and possess very high polarization fields ( $\sim$ MV/cm) along the common growth direction of  $\langle 0001 \rangle$ . Such large polarization fields lead to undesired shifts (e.g., wavelength and current) in the performance of photonic and vertical transport electronic devices. The cubic phase of GaN materials is polarization-free along the common growth direction of  $\langle 001 \rangle$ , however, this phase is thermodynamically unstable, requiring low-temperature deposition conditions and unconventional substrates (e.g., GaAs). Here, novel nano-groove patterning and maskless selective area epitaxy processes are employed to integrate thermodynamically stable, stress-free, and low-defectivity c-GaN on CMOS-compatible on-axis Si. These results suggest that epitaxial growth conditions and nano-groove pattern parameters are critical to obtain such high quality c-GaN. InGa<sub>x</sub>GaN/GaN multi-quantum-well structures grown on c-GaN/Si (100) show strong room temperature luminescence in the visible spectrum, promising visible emitter applications for this technology.

ones to inherently polarization-free (a.k.a. nonpolar) ones. Practically, most common nonpolar substrate is the m-plane free-standing GaN one (i.e. making  $90^\circ$  with the respect to  $\langle 0001 \rangle$  direction) that are sliced along  $\{1100\}$  planes out of GaN boules grown along  $\langle 0001 \rangle$  direction.<sup>[4]</sup> Hence, m-plane substrates are small area ( $\sim$ cm<sup>2</sup>) and expensive. Moreover, (1) high quality epitaxial regrowth of GaN on nonpolar surfaces is challenging due to low surface energy of nonpolar planes,<sup>[5]</sup> and (2) indium incorporation into In<sub>x</sub>Ga<sub>(1-x)</sub>N (the visible LED active layers where  $0.05 < X < 0.35$ ) is significantly degraded for nonpolar structures<sup>[6]</sup> limiting the promise of such substrates in visible LEDs and laser diodes (LDs) applications.

An alternative way of enabling polarization-free GaN devices is through controlling the material phase. Conventionally-grown GaN material is hexagonal (wurtzite) phase which is polar along

$\langle 0001 \rangle$  growth direction. However, GaN material can also be cubic (zinc blende) phase which is polarization-free along  $\langle 001 \rangle$  growth direction.<sup>[7]</sup> Nonetheless, cubic phase of GaN is observed to form when grown on cubic substrates such as GaAs. Thermodynamical instability of cubic phase GaN, epilayer-substrate chemical incompatibility (i.e. III-N vs. III-As), and large lattice-mismatch (i.e.  $\sim 20\%$ ) are some of the key issues bottlenecking such bulk epitaxial deposition schemes.<sup>[8]</sup>

Additional key motivation to our work is the GaN-Si(100) integration that presents further advantages such as on-chip photonics and availability of cleavage.<sup>[9,10]</sup> However, anisotropic lattice-mismatch (i.e.  $\sim 14\%$  GaN  $\langle 11\bar{2}0 \rangle \parallel$  Si  $\langle 100 \rangle$  and  $\sim 0.6\%$  for GaN  $\langle 10\bar{1}0 \rangle \parallel$  Si  $\langle 100 \rangle$ ) and crystallographic asymmetry (i.e. (wurtzite GaN (0001)) six fold versus fourfold (Si(100))) leads to different rotational crystals of GaN grow on Si(100) surface.<sup>[11]</sup> These lead GaN epilayers suffer from twist boundaries and low quality epitaxy. Thus, offcut-oriented Si(100) substrates (typically  $4^\circ$  to  $7^\circ$  towards (110)) are preferred for single crystal-line GaN epitaxy.<sup>[12]</sup> However, for true integration with silicon electronics, it is essential to develop GaN epitaxy on on-axis Si(100) substrates as offcut in silicon substrates lead to anisotropy and performance issues in silicon electronic devices.<sup>[13]</sup>

We have addressed such integration issues of GaN on on-axis Si (100) substrates by (1) employing a unique nanopattern on CMOS-compatible Si substrate that expose a U-shaped

## 1. Introduction

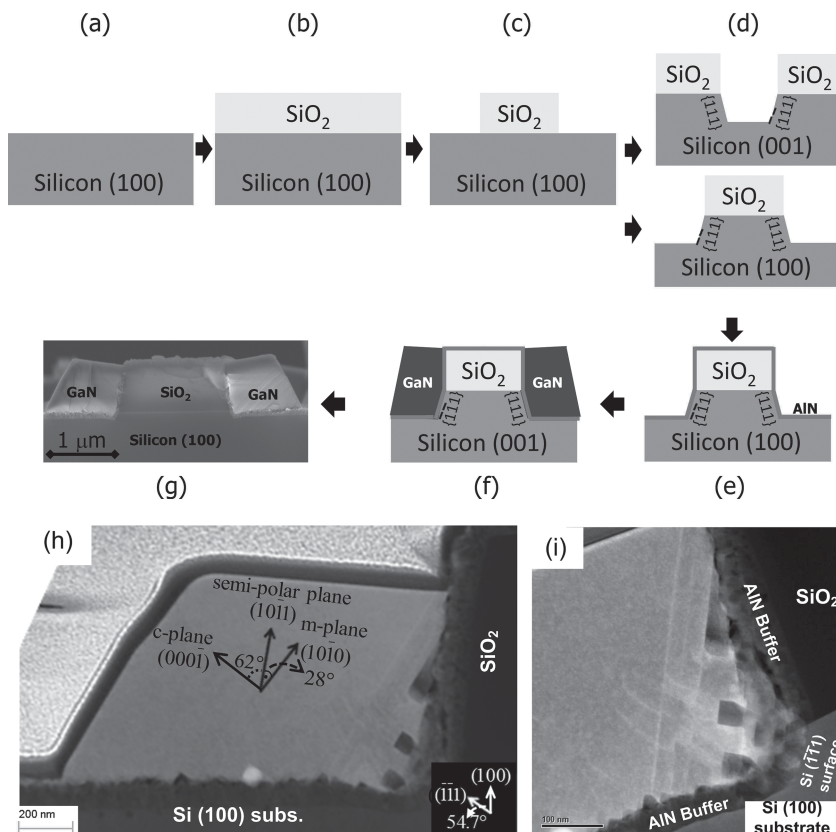
GaN materials (i.e. III-nitrides) are the backbone materials of light emitting diodes (LEDs) emitting in the ultraviolet, blue, and green spectra. LED layers, grown on conventional sapphire and silicon carbide substrates, are hexagonal (i.e. wurtzite) phase and possess inherit polarization fields along the common growth direction  $\langle 0001 \rangle$ .<sup>[1]</sup> However, recent studies showed polarization fields to contribute droop phenomena in LEDs<sup>[2]</sup> and I-V hysteresis in resonant tunneling diodes.<sup>[3]</sup> Thus, it is essential to focus on polarization-free designs to improve GaN photonic and vertical transport device performances.

Conventional approach to enable polarization-free GaN devices is switching the growth plane from inherently polar

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**Figure 1.** Schematic process flow for (a–d) silicon (100) substrate preparation and (e–f) MOCVD growth processes: (a) RCA cleaning; (b) thermal oxide ( $\text{SiO}_2$ ) growth; (c) deep ultraviolet (193 nm) lithography and reactive ion etching of oxide ( $\text{SiO}_2$ ); (d) KOH dip (10%) to create the final groove structures: (top)  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}\text{-Si}\{111\}\text{-SiO}_2]$  or (bottom)  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}]$ ; (e) Low temperature AlN buffer deposition, (f) high temperature GaN layer deposition. (g–i) Cross-section views of wurtzite phase GaN grown: (g) SEM and (h) HAADF-STEM view with crystallographic directions, and (i) HAADF-STEM view zoomed in GaN $\{000\bar{1}\}$ -Si $\{\bar{1}\bar{1}1\}$  interface highlighting the stacking faults and dislocation-filtering due to trench growth mode. The GaN growth is initiated on the exposed Si  $\{111\}$  planes of patterned Si (100) substrate.

groove exposing both Si  $\{111\}$  and Si $\{100\}$  planes, and (2) developing a truly selective GaN-regrowth scheme that deposits GaN selectively on Si  $\{111\}$  facets rather than Si  $\{100\}$  ones. Besides, a unique phenomenon is observed when two h-GaN growth fronts met in our novel groove structure leading to c-GaN regrowth after seam.

## 2. Results and Discussion

**Figure 1** shows the schematic process flow for silicon (100) substrate preparation prior to MOCVD growth. First, CMOS-compatible on-axis Si (100) substrate is cleaned via standard RCA process. Then, 500-nm-thick thermal oxide ( $\text{SiO}_2$ ) is grown, followed by deep ultraviolet (193 nm) lithography. Subsequently, reactive ion etching of oxide ( $\text{SiO}_2$ ) is realized to expose Si (100) surface on parts of the wafer. After another RCA-like cleaning process, the wafer is submersed into KOH (10%) solution for ~1 min to selectively etch Si and expose  $\{111\}$  facet family. By this approach, two different groove

structures  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}]$  and  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}\text{-Si}\{111\}\text{-SiO}_2]$  are formed on on-axis Si (100) parent substrate, as shown in Figure 1d. After desired groove structures are formed and surface native oxide is removed via dilute HF treatment, wafers are loaded inside the MOCVD chamber for growth.

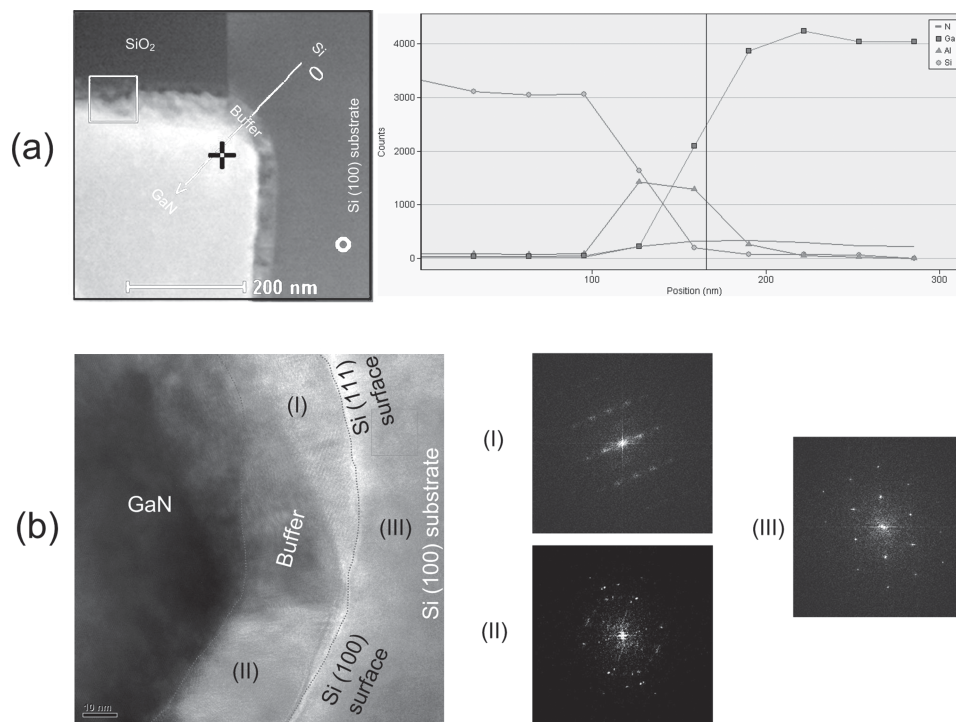
Figure 1g and Figure 1(h,i) show cross-sectional scanning electron microscope (SEM) and high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) images of h-GaN, respectively, grown on  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}]$  groove structures. The crystallographic directions for h-GaN and Si are displayed in Figure 1h. We have identified the crystallographic directions from the known fact that GaN (0001) growth direction is the same as Si (111) ones, and from our experimental observations that GaN regrowth is nucleated from Si  $\{111\}$  facets only. Given these two, we have used SEM and transmission electron microscope (TEM) to identify the angles between the observed facets of GaN. As wurtzite phase GaN c-plane is along the Si  $\{111\}$ , top GaN facet, making an angle of ~62° and 28° with GaN c- and m-planes, respectively, is determined to be semi-polar ( $10\bar{1}1$ ) plane (see supplementary materials and Figure S1 for crystal directions and planes).<sup>[14]</sup>

SEM and TEM results show that low temperature (~700 °C) AlN buffer was deposited everywhere (on all Si planes and  $\text{SiO}_2$ ). This is due to high sticking coefficient of Al adatom and employment of low growth temperatures for the buffer. However, GaN regrowth atop AlN buffer is determined to nucleate from Si( $\bar{1}\bar{1}1$ ) surface as shown in

Figure 1i. SEM and TEM are employed to verify that no kind of GaN regrowth or deposition were on the Si  $\{100\}$  facets. This is attributed to optimized MOCVD growth conditions enabling selective nucleation of GaN on Si (111) surfaces rather than Si (100) ones (see supplementary materials and Figures S2–S3). Mainly, our selective MOCVD scheme consists of four steps: (1) Ammonia-free heat up, (2) Prealuminization, (3) AlN buffer deposition, and (4) GaN layer deposition.

Having a  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}]$  trench, GaN growth along the c-direction ( $000\bar{1}$ ) seems further complicated with void formations.<sup>[15,16]</sup> Figure 1i shows the TEM image zoomed in at the GaN-Si interface where partially-filled voids (the dark regions in Figure 1i) and stacking faults (white lines in Figure 1i) along the m-plane ( $10\bar{1}0$ ) are observed. Interestingly, as growth front (c-plane) is perpendicular to stacking faults (m-plane), these stacking faults filter the threading dislocations (TDs). Hence, XTEM data reveals no discernable TDs reaching to the top-most GaN surface.

We have further studied the GaN $\{000\bar{1}\}$ -Si  $\{\bar{1}\bar{1}1\}$  interface to understand mechanisms of such growth selectivity. TEM



**Figure 2.** (a) TEM chemical analysis performed through the GaN{000 $\bar{1}$ }-Si{ $\bar{1}\bar{1}$ 1} interface (along the red arrow line). Significant Si diffusion into the AlN buffer layer is observed. (b) HR-TEM image of the GaN{000 $\bar{1}$ }-Si{ $\bar{1}\bar{1}$ 1} interface highlighting a structural difference between the buffer layer on Si(111) and Si(100) surfaces. Red freeform curves are drawn to guide for the buffer layer region. FFT diffraction patterns from selected area regions (I), (II), and (III) are shown (electron beam is parallel to  $[1\bar{1}20]$  zones of h-GaN). Regions (I), (II), and (III) are observed to be wurtzite single crystalline, polycrystalline, and diamond single crystalline.

chemical line and high resolution TEM (HR-TEM) analyses are carried out along the GaN-Buffer-Si interfaces. For buffer layers on Si(111) surfaces, high Si diffusion into the AlN buffer and single crystalline buffer material is observed (see **Figure 2**). However, for buffer layers on Si(100) surfaces, this was not the case (see supplementary materials and Figure S4). FFT diffraction patterns reveal that the AlN buffer on Si(111) surface is single crystalline in hexagonal (wurtzite) phase whereas that on Si(100) surface is polycrystalline (see Figure 2b). We believe selective GaN growth on Si(111) surfaces is due to this difference in the crystallinity of the corresponding buffer layer.

We have then carried out GaN regrowth on  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}\text{-Si}\{111\}\text{-SiO}_2]$  groove structures (depicted in **Figure 3a**) under aforementioned selective growth conditions. Such groove structures with short periods are of particular interest to increase effective GaN epitaxial coverage on Si(100) substrate without the expense of growth time as well as may reduce significant wafer bow typically encountered in conventional epitaxy due to the coefficient of thermal expansion (CTE) mismatch between GaN and Si.

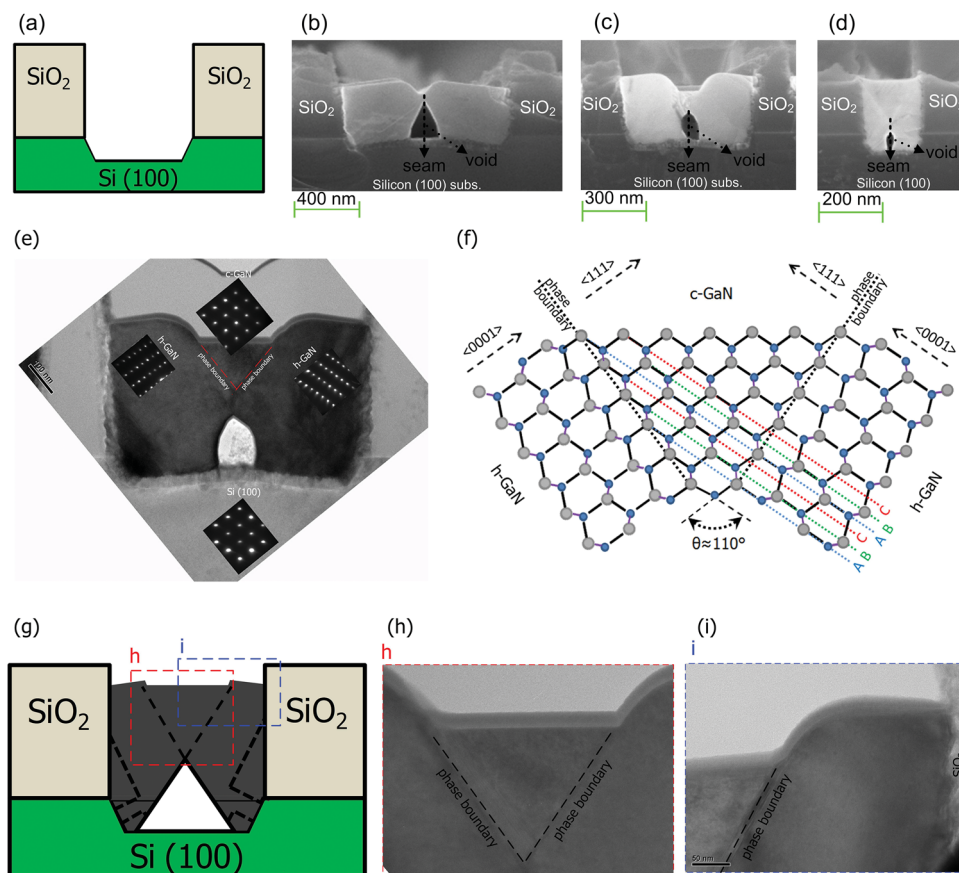
Under selective MOCVD growth conditions, GaN regrowth is nucleated on the Si{111} family of planes rather than Si{100} ones, as shown earlier. Thus,  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}\text{-Si}\{111\}\text{-SiO}_2]$  groove structures have only two nucleation sites for GaN regrowth: Si(111) and Si( $\bar{1}\bar{1}$ 1) surfaces. When GaN growth fronts initiated from facing directions meet, a void is formed in the middle where the seam forms (Figures 3 and S5).

The size of the void depends on the groove period as well as the growth parameters.<sup>[17]</sup> Figure 3(b–d) shows the cross-sectional SEM of partially-GaN-filled groove structures with openings of (b) 1000 nm, (c) 650 nm, and (d) 250 nm. Interesting, two distinct features are observed at seam: voids and crystallographic faults.

Figure 3 shows the bright-field TEM of a groove structure. Figure 3h shows bright-field TEM image zoomed around the seam area. These TEM data shows that some intersecting crystallographic faults are initiated at seam forming a triangular region (see Figure 3f for the exploratory sketch and supplementary materials for Figure S6). To understand the nature of such faults, Fast Fourier transform (FFT) technique is employed to check and determine GaN crystalline phase inside and outside the triangular region.

Selective area electron diffraction patterns are shown in Figure 3e. Diffraction patterns from the exact regions and the orientation of the sample have been maintained. These different diffraction patterns correspond to wurtzite and cubic phase crystallographic electron diffractions of GaN, respectively, given that the TEM data was taken with electron beam parallel to  $[1\bar{1}20]$  zone of wurtzite phase GaN (that corresponds to  $[1\bar{1}0]$  zone of cubic phase GaN) (see Figure S7).<sup>[18,19]</sup> Thus, crystallographic faults initiated at the seam are identified to be phase boundaries. Bright-field TEM images in Figure 3 reveal no threading dislocations on both c-GaN and h-GaN surfaces. Authors believe phase boundaries circumscribing the cubic phase GaN (V-shape alike) help suppress





**Figure 3.** (a) Cross-sectional sketch of a  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}\text{-Si}\{111\}\text{-SiO}_2]$  groove structure used for GaN regrowth. (b–d) Cross-sectional SEM of GaN grown on grooved Si (100) substrate having openings of (b) 1000 nm, (c) 650 nm, and (d) 250 nm. (e) Cross-sectional bright-field TEM of a partially-GaN-filled groove structure. FFT diffraction patterns from the boxed regions shown correspond to c-GaN, h-GaN, and Si (100) (see supplementary materials). Diffraction patterns from the exact regions and the orientation of the sample have been maintained. Electron beam is parallel to  $[11\bar{2}0]$  and  $[1\bar{1}0]$  zones of wurtzite and cubic phase GaN, respectively. (f) Cross-sectional sketch depicting wurtzite to cubic phase transition observed in the groove. (g) Cross-sectional sketch of a partially-GaN-filled groove structure. (h,i) Bright-field TEM images of (h) c-GaN and (i) h-GaN surfaces revealing no threading dislocations.

TDs propagation as cubic phase growth front is aligned with  $\text{Si}[100]$  direction whereas wurtzite phase growth front is aligned with  $\text{Si}[111]$ .

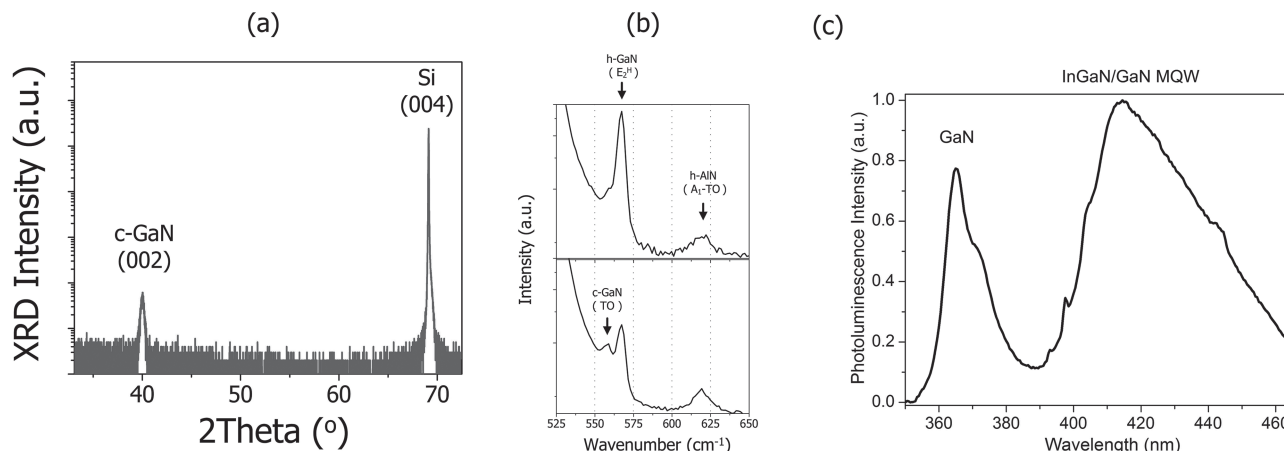
X-ray diffraction (XRD) studies are carried out to verify the phase of GaN grown on  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}\text{-Si}\{111\}\text{-SiO}_2]$  groove structure. Omega/2Theta XRD data shown in Figure 4a reveals a peak at  $\sim 40^\circ$  corresponding to the cubic phase of GaN. Room temperature Micro-Raman measurements are carried out for GaN on  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}]$  and  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}\text{-Si}\{111\}\text{-SiO}_2]$  groove structures (see Figure 4b). We observed only h-GaN peak for the former whereas the latter showed a c-GaN peak as well. Interestingly, comparing the Raman peak locations of h-GaN and c-GaN on grooved Si (100) with the literature,<sup>[20,21]</sup> one can conclude that these materials are stress-free (freestanding GaN Micro-Raman spectrum provided in Figure S9). Authors believe this is due to the localized epitaxy process rather than conventional bulk deposition.

As XTEM data identified no discernable TDs reaching to the cubic-phase GaN surface, we have grown three period InGaN/GaN multi-quantum-well (MQW) active layer on such cubic phase GaN on  $[\text{SiO}_2\text{-Si}\{111\}\text{-Si}\{100\}\text{-Si}\{111\}\text{-SiO}_2]$  groove

structures. Figure 4(c) shows the room temperature photoluminescence (PL) measurement data. Intense ultraviolet and blue luminescence are observed from GaN and InGaN/GaN MQW, respectively, proving the optical quality of the regrown layers on cubic phase GaN.

### 3. Conclusions

CMOS-compatible integration of wurtzite and cubic phase GaN on on-axis Si (100) substrates are realized through novel nano-groove pattern and selective MOCVD process. XTEM data shows no discernable threading dislocations on the h- and c-GaN surfaces. InGaN/GaN MQWs regrown on c-GaN templates demonstrated strong room temperature emission in blue spectrum. GaN wurtzite to cubic phase transition can be particularly beneficial for light emitting devices as GaN cubic phase is nonpolar and polarization-free. Our MOCVD growth technique and unique groove structure are particularly beneficial for integrating GaN devices with Si CMOS technology (see Figure S9).



**Figure 4.** (a) Omega/2Theta XRD scan of GaN on a [SiO<sub>2</sub>-Si{111}-Si{100}-Si{111}-SiO<sub>2</sub>] groove structure showing cubic phase diffraction peak. (b) Room temperature Micro-Raman spectra of (top) GaN on [SiO<sub>2</sub>-Si{111}-Si{100}] groove structure (seen in Figure 1(h)) and (bottom) GaN on a [SiO<sub>2</sub>-Si{111}-Si{100}-Si{111}-SiO<sub>2</sub>] groove structure (seen in Figure 3(e)). The former has only h-GaN whereas the latter shows additional c-GaN peak. (c) Room temperature PL spectrum of InGaN multi-quantum-wells grown on GaN on a [SiO<sub>2</sub>-Si{111}-Si{100}-Si{111}-SiO<sub>2</sub>] groove structure. Strong ultraviolet and blue luminescence are observed from GaN and InGaN/GaN multi-quantum-wells, respectively.

## 4. Experimental Section

Our optimal MOCVD condition consists of a four step approach: (1) Ammonia-free heat up (~5–10 min) to prevent Si surface nitridation and remove any native oxide, (2) long-enough prealuminumization via introducing only TMAl into the chamber to aluminumize the Si surface (at least 10 s) prior to any deposition, (3) thick-enough AlN buffer deposition (at least 60-nm-thick deposited at 700 °C) prior to GaN deposition, and (4) high temperature GaN regrowth (at a temperature of ≥1150 °C). Such optimized MOCVD parameters enable a uniform and controlled GaN regrowth (Figure S2 right) over that under conventional conditions (Figure S2 left).

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